Lierda MB26-A Y0C Series Hardware Design Manual

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Revision History

Document version	Change date	Reviser	Reviewer	Change content
Rev1.0	23-05-05	CZT	SLY，YMX	Initial version
Rev1.1	23-09-08	CZT	SLY，YMX	Update RF performance and power consumption data.
Rev1.2	24-08-02	CZT		Update module top view
Rev1.3	24-10-29	HKJ		Add precautions to avoid mercury or mercury vapor in module production and use.
Rev1.4	24-12-10	HKJ		Modify the module packaging description of the key features; modify the description related to the default voltage level of VDD_EXT, suitable for adding the new model MB26-A Y0C-Q-B01 to the module.
Rev1.5	24-12-11	HKJ		RI and NETLIGHT functions are not supported by default and need to be enabled via software.
Rev1.6	25-02-21	HKJ		Update the description related to PSM_EINT0.
Rev1.7	25-04-29	CZT		Add a section titled "1.1 Special Characters" Update the description of the key feature table module weight. Change the format of the note content Update the electrical characteristics of the power interface in Table 6-2. Adjust operating and storage temperature to section 6.6.

Safety Instructions

Users are responsible for complying with the relevant regulations on wireless communication modules and devices in other countries, as well as specific environmental regulations for use. By following the following safety principles, personal safety can be ensured and help protect products and work environments from potential damage. Our company is not responsible for any losses resulting from customers' failure to comply with these regulations.

	Road safety comes first! When driving, please do not use handheld mobile devices unless they have hands-free functionality. Please park your car before making a call!
	Please turn off your mobile devices before boarding. The wireless function of mobile devices is prohibited on the plane to prevent interference with the aircraft communication system. Ignoring this prompt may jeopardize flight safety and even violate the law.
	When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference can cause medical equipment to malfunction, so it may be necessary to turn off mobile terminal devices.
	Mobile terminal devices do not guarantee effective connection in all situations, such as when the mobile terminal device is out of credit or the SIM card is invalid. In case of emergencies under the above circumstances, remember to use emergency calls, and ensure that your device is powered on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and transmit radio frequency signals when powered on, which may cause radio frequency interference when near a TV, radio, computer, or other electronic devices.
	Please keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off the mobile terminal devices. Operating electronic devices in any potentially explosive environment poses a safety hazard.

Module selection for application.

Serial number	Module model	Feature symbol	Support frequency bands	Dimensions	Module Introduction
1	MB26-A	Y0C-Y-B01	Band3/5/8	15.8×17.7×2.2(mm)	VDD_EXT voltage level is default 3.3V
2	MB26-A	Y0C-X-B01	Band3/5/8	15.8×17.7×2.2(mm)	VDD_EXT level defaults to 3.0V.
3	MB26-A	Y0C-Q-B01	Band3/5/8	15.8×17.7×2.2(mm)	VDD_EXT voltage level defaults to 1.8V

Content

1 Introduction

This document defines the application specifications of the Lierda MB26-A Y0C series NB-IoT module, describing its hardware interface, electrical characteristics, application methods, and mechanical specifications, among other content.

This document can help users quickly understand the hardware interface specifications, electrical, mechanical characteristics, and other related information of the module. Combined with other relevant documents, users can quickly grasp the application methods of the NB-IoT module.

1.1 Special characters

Table 1-1 Special Symbol Description

Symbol	Definition
※	Unless otherwise specified, the asterisk (*) marked after the module functions, features, interfaces, pin names, AT commands, or parameters indicates that the development of the module's function, feature, interface, pin name, AT command, or parameter is in progress and not yet supported.

2 Product Overview

The MB26-A Y0C series module is a leading NB-IoT wireless communication module globally, compliant with 3GPP standards, supporting Band03, Band05, Band08 frequency bands. It features small size, low power consumption, long transmission distance, strong anti-interference ability, etc. Using this module, customers can easily and flexibly conduct product design, such as smart meter reading, smart parking, smart cities, smart security, asset tracking, smart home appliances, agriculture, and environmental monitoring.

2.1 Frequency bands and functions

The MB26-A Y0C mentioned in this document represents the general term for this series model, Table 2-1 provides some Band descriptions supported by the module.

Table 2-1 Partial Band Description Supported by the Module

Frequency Band Band	Uplink frequency band Uplink(UL)band	Downlink frequency band Downlink(DL)band	Network standard Duplex Mode
Band3	1710MHz-1785MHz	1805MHz-1880MHz	H-FDD
Band5	824MHz-849MHz	869MHz-894MHz	H-FDD
Band8	880MHz-915MHz	925MHz-960MHz	H-FDD

2.2 Key features

The table below shows the key features of the product:

Table 2-2 Module Key Features Description

Parameters	Explanation
Module packaging	LCC
Ultra-small module size	(17.7±0.15)×(15.8±0.15)×(2.2±0.2)mm(L×W×H)
Module weight	About 1.1 grams

Ultra-low power	1.5uA@PSM
Operating voltage	◆ Normal operating voltage range: 2.2~4.5V(1) ◆ Expand working voltage range: 2.1~4.5V
Operating temperature	Operating temperature range: -40~85°C
Storage temperature	Storage temperature range: -40 to 90°C
Transmit power	23dBm±2.7dB(Max)
USIM interface	Provide external SIM card interface, support 1.8/3.0V USIM card.
Serial port	Main Serial Port: ◆ Used for AT command transmission and data transfer, the supported baud rate defaults to 9600 bps. For more details, Please refer to section 4.1. ◆ Used for firmware upgrade. Debug serial port: ◆ Assist in troubleshooting some abnormal restarts, network issues, and application protocol problems in conjunction with debugging tools. ◆ The default baud rate of the serial port is 3Mbps.
Communication interface characteristics	Support 3GPP Rel.13/14 NB-IoT wireless radio communication interface and protocol
Features of network protocols	Embedded TCP/IP, UDP/IP, LWM2M and other network protocol stacks.
Data transmission characteristics(4)	◆ Single-Tone (Max): 25.5 kbps (Downlink); 16.7 kbps (Uplink) ◆ Multi-Tone (Max): 127 kbps (downlink); 158.5 kbps (uplink)
Firmware upgrade	◆ Main serial port upgrade ◆ DFOTA upgrade
Antenna Interface	50 ohm characteristic impedance
RoHS	All components comply with EU RoHS standards.

Note

(1) See section 6.2 for a specific description of the expansion voltage.

(2)(3) See section 6.3 for specific descriptions regarding temperature.

The data transmission rate is theoretical.

2.3 Function Diagram

The following is the product function block diagram:

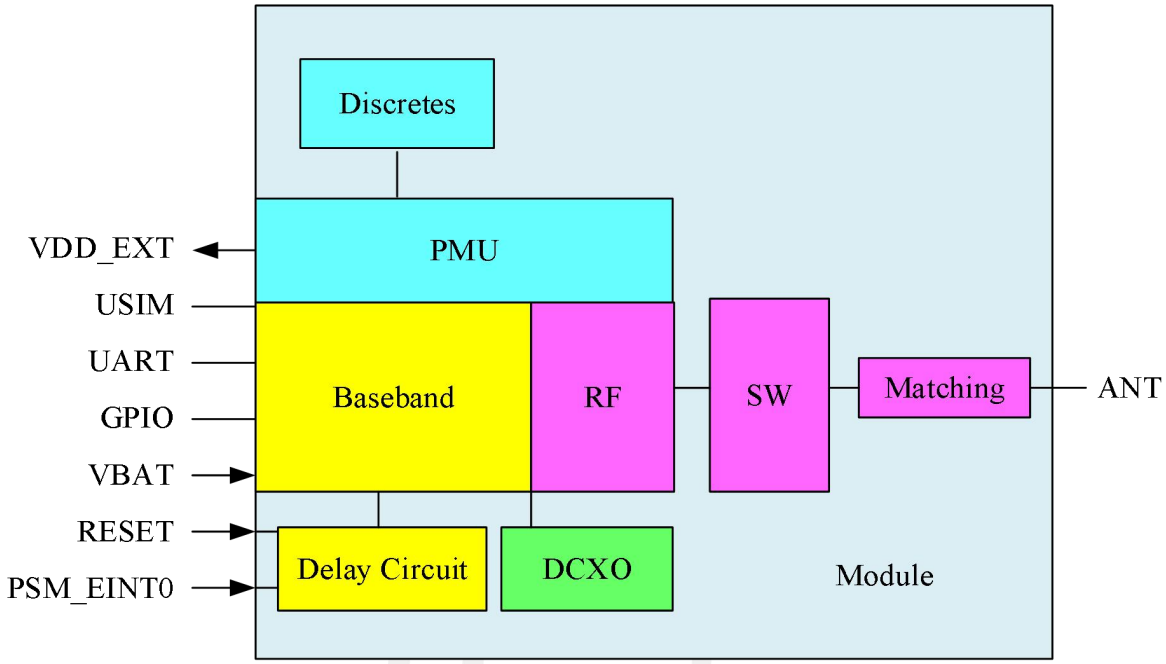


Figure 2-1 Functional Block Diagram

2.4 Pinout diagram

The MB26-A Y0C module has a total of 44 LCC pins:

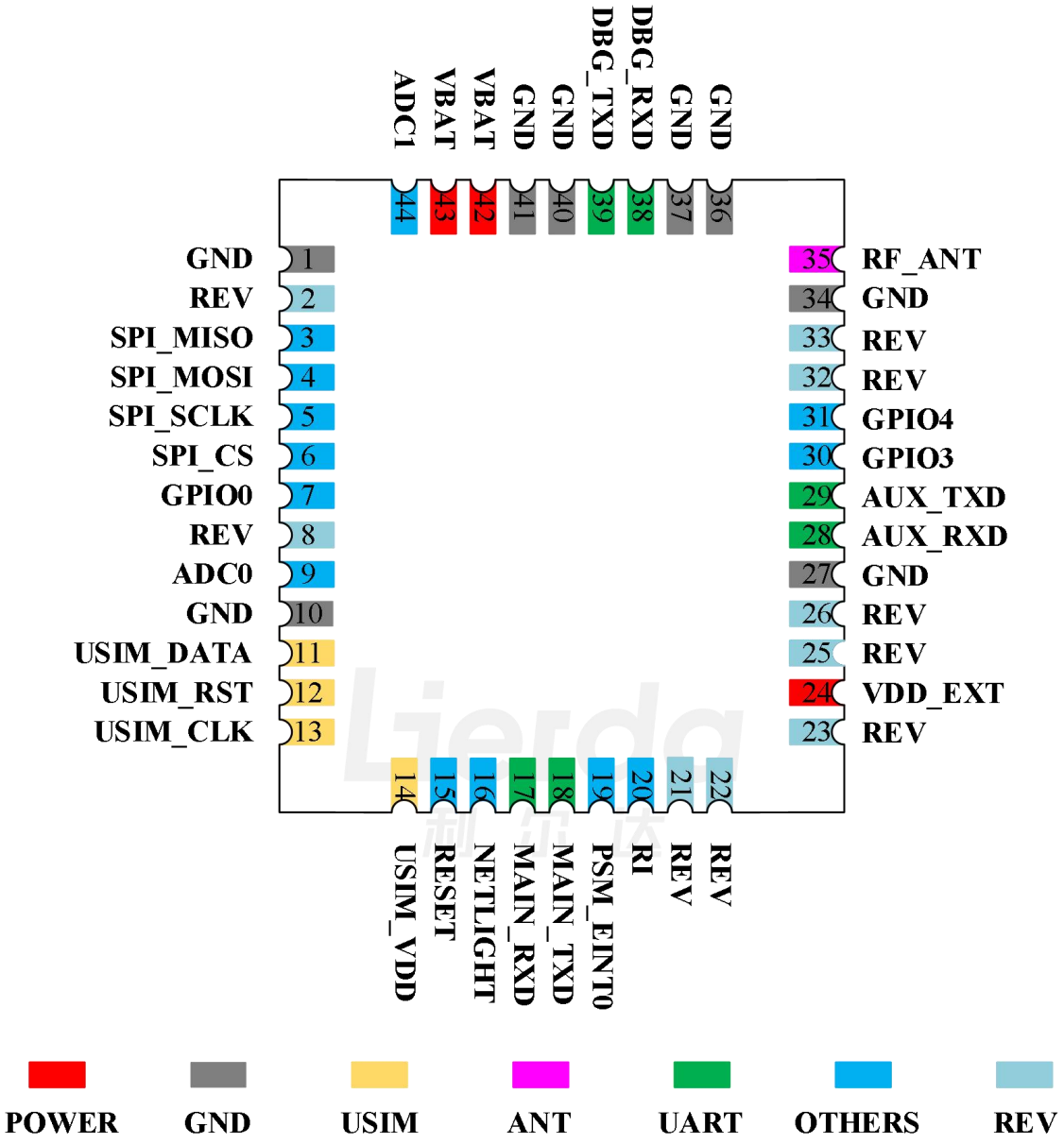


Figure 2-2 Pin Assignment Diagram (for MB26-A Y0C series)

2.5 Pin Description Table

For better understanding of the application, the following is an explanation of the types of I/O parameters in the table:

Table 2-3 Definition Explanation of I/O Parameters

I/O parameters Type	Explanation
IO	Input Output
DI	Numeric input
DO	Number output
PI	Power input
PO	Power output
AI	Simulated Input
AO	Simulated output

For better understanding of the application, the following table provides a description of the characteristics of the power domain parameters:

Table 2-4 Module Power Domain Characteristics Description

Power domain parameters Type	DC characteristics	Explanation	Power supply object
VBAT	Vmax=4.5V Vmin=2.1V Vnorm=3.6V	Module power input, recommended to use 3.6V/0.5A power supply.	Module
VO_LDOIO	VILmax=0.2×VO_LDOIO VIHmin=0.7×VO_LDOIO VOLmax=0.15×VO_LDOIO VOHmin=0.8×VO_LDOIO	Configurable from 1.8V to 3.3V, with different default voltage levels for different models, Y0C-Y defaults to 3.3V, Y0C-X defaults to 3.0V, Y0C-Q defaults to 1.8V. Maximum driving capability is 120mA; In PSM mode, when configured in any one of the three power consumption modes: Sleep Mode 1,	UART GPIO VDD_EXT

		Sleep Mode 2, Hibernation, VO_LDOIO=0V, the associated IO port will also be powered off.	
VDD18AON	VILmax=0.2×VDD18AON VIHmin =0.75×VDD18AON	In PSM mode, no power off, see sections 3.5 and 3.6 for details.	RESET PSM_EINT0
VO_LDOSIM	Vnorm=1.8/3.0V VOLmax=0.15×VO_LDOSIM VOHmin=0.8×VO_LDOSIM VILmax=0.2×VO_LDOSIM VIHmin=0.7×VO_LDOSIM	SIM card dedicated power supply, supporting 1.8/3.0V card	USIM

Table 2-5 Module Pin Description

1. Power					
Pin number	**Pin Names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
42,43	VBAT	PI	Power supply	VBAT	Refer to Table 2-4.
24	VDD_EXT	PO	Reference level output	VO_LDOIO	See Table 2-4
1,10,27, 34,36,37 40,41	GND		GND		

2. RESET					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
15	RESET	DI	Reset module	VDD18AON	Low level effective

3. Wake up PSM_EINT0					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
19	PSM_EINT0	DI	External wake-up module	VDD18AON	Low level effective

4. Network status indicator					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
16	NETLIGHT※	DO	Network status indicator	VDD18AON	

5、ADC interface					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
9	ADC0	AI	Analog-to-Digital Conversion	Internal direct connection Input voltage range: 0~1.6V Internal voltage divider Input voltage range: 0~3.6V	Default 1.6V Internal voltage division can be enabled through software.
44	ADC1	AI	Universal Modulus Conversion		

6. Serial Port UART					
Pin number	**Pin Names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
17	MAIN_RXD	DI	Main Serial Port: Module receives data	VO_LDOIO	Important: Under PSM, the main serial port RXD will automatically switch to the VDD18AON power domain, while other serial ports will be powered off. Please set the working mode of RXD according to the actual
18	MAIN_TXD	DO	Main Serial Port: Module sends data		
38	DBG_RXD	DI	Debugging serial port: Module receives data		
39	DBG_TXD	DO	Debugging serial port: Module sends data		
28	AUX_RXD	DI	Serial Port Application: Module receives data		
28	AUX_TXD	DO	Serial Port Application:		

			Module sends data		situation, refer to section 4.1 for details.

7. External USIM card interface					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
11	USIM_DATA	IO	SIM card data cable	VO_LDOSIM	Please refer to section 4.2.
12	USIM_RST	DO	SIM card reset line		
13	USIM_CLK	DO	SIM card clock line		
14	USIM_VDD	PO	SIM card power supply		

8. Antenna interface RF					
Pin number	**Pin names**	**I/O**	**Description**	**DC characteristics**	**Note**
35	RF_ANT	IO	RF antenna interface	50Ω characteristic impedance	Please refer to Chapter 5.

9. General Purpose IO Interface					
Pin number	**Pin names**	**I/O**	**Describe**	**Power Domain/DC Characteristics**	**Note**
7	GPIO0	IO	Internal connect GPIO0	VO_LDOIO	
30	GPIO3	IO	Internal connect GPIO13		
31	GPIO4	IO	Internal connect GPIO14		

10. SPI Interface					
Pin number	**Pin Names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
3	SPI_MISO	DI	SPI master input, slave output	VO_LDOIO	
4	SPI_MOSI	DO	SPI master output		

			from input		
5	SPI_SCLK	DO	SPI serial clock		
6	SPI_CS	DO	SPI chip select		

11. RI Interface					
Pin number	**Pin names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
20	RI※	DI	Ringing signal	VO_LDOIO	

12. Reserve interface					
Pin number	**Pin Names**	**I/O**	**Description**	**Power Domain/DC Characteristics**	**Note**
2,8,22,23, 26,32,33	REV		TBD		Undefined, please keep suspended when in use.

2.6 Evaluation Suite

Lierda can provide a complete evaluation and development kit, including development boards with USB interfaces. Feel free to contact us for more information.

3 Characteristics of work

3.1 Working mode

The table briefly describes the three states of the module under normal operating mode.

Table 3-1 Three States in Working Mode

Pattern	Status	Status Description
Working mode	Active	The module is in active state; all functions are working properly and available for data transmission and reception; the module can switch to Idle mode or PSM mode in this state.
	Idle	The module is in a shallow sleep state, the network is in a connected state, and can receive paging messages. The module can switch to active mode or PSM mode in this mode.
	PSM	The module only has the RTC working, the network is in a disconnected state, and no longer accepts paging messages. The module will be awakened when the DTE (Data Terminal Equipment) actively sends data or when the timer T3412 (periodic update) times out.

Different from the three states (Active, Idle, PSM) under the NB working mode, the module also supports multiple power saving modes, each of which can be configured via AT commands.

The former is the operating status of the NB protocol, and the latter is the power consumption mode of the module itself.

The former is determined by the network, while the latter can be freely configured by the user.

Table 3-2 Power Consumption Mode Types and Configuration

Power consumption mode	AT configuration command	Status description
Operating mode	AT+ECPMUCFG=1,0	Without activating the low power mode, even when there is nothing to do, the module MCU remains in a loop waiting state, consuming a significant amount of power.
Idle mode	AT+ECPMUCFG=1,1	The module MCU will shut down the core working clock

		when there is no task, and any interrupt can wake up the system and restart the core clock.
Sleep mode 1	AT+ECPMUCFG=1,2	On the basis of idle mode, all external devices are powered off, and the content of 256KB/16KBSRAM is maintained, external interrupts cannot wake up the system.
Sleep Mode 2	AT+ECPMUCFG=1,3	Disable 256KBSRAM and keep only 16KB SRAM on the basis of sleep mode 1.
Hibernation	AT+ECPMUCFG=1,4	On the basis of Sleep mode 2, turn off the 16KBSRAM. (SRAM does not retain content)

3.2 Hibernate mode

The main purpose of PSM is to reduce module power consumption and extend the battery's supply time. The figure below shows the power consumption of the module in different modes.

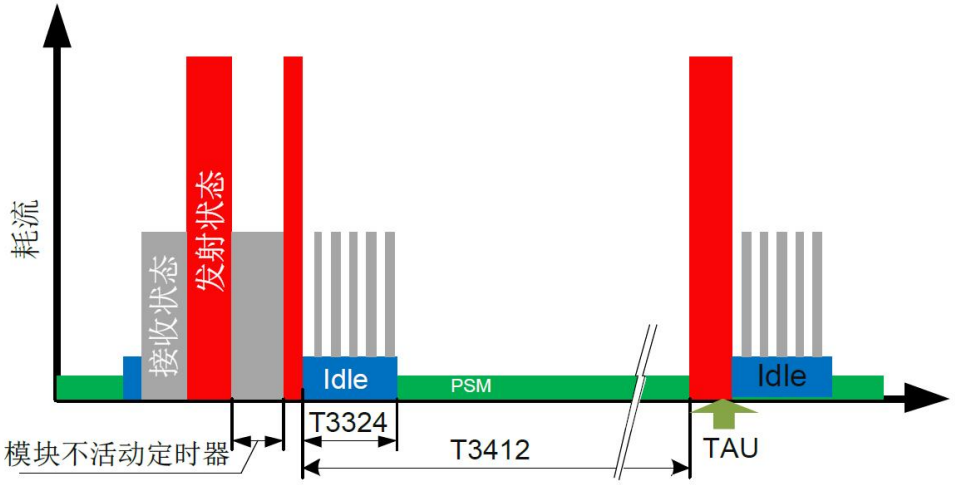


Figure 3-1 Functional Block Diagram

The process of module entering PSM is as follows: When the module establishes a connection with the network side or updates the Tracking Area Update (TAU), it will request to enter PSM in the request message. The network side will configure the T3324 timer value in the response message to the module and start the Reachable Timer. When the T3324 timer expires, the module enters PSM. The module cannot request to enter PSM

when connecting for emergency services or initializing public data networks.

When the module is in PSM, the network activities will be disabled, including searching for cell messages, cell reselection, etc. However, the T3412 timer (related to periodic TAU updates) will still continue to work.

The module can exit PSM in the following two ways:

- DTE actively sends data to exit PSM.
- When the T3412 timer times out, the Tracking Area Update (TAU) is triggered, and the module exits the Power Saving Mode (PSM).

In PSM state, users can configure three power consumption modes according to their needs: Sleep Mode 1, Sleep Mode 2, and Hibernation Mode.

3.3 Power supply design

The MB26-A Y0C series module provides 2 VBAT pins for connecting external power sources, the interface description is as follows:

Table 3-3 Power Supply Pin Definitions

Pin number	Pin names	I/O	Description	Note
42,43	VBAT	PI	Power supply	The power supply must be able to provide a current of up to 0.5A.
1,10,27,34, 36,37,40,41	GND		GND	

3.3.1 Power circuit reference design

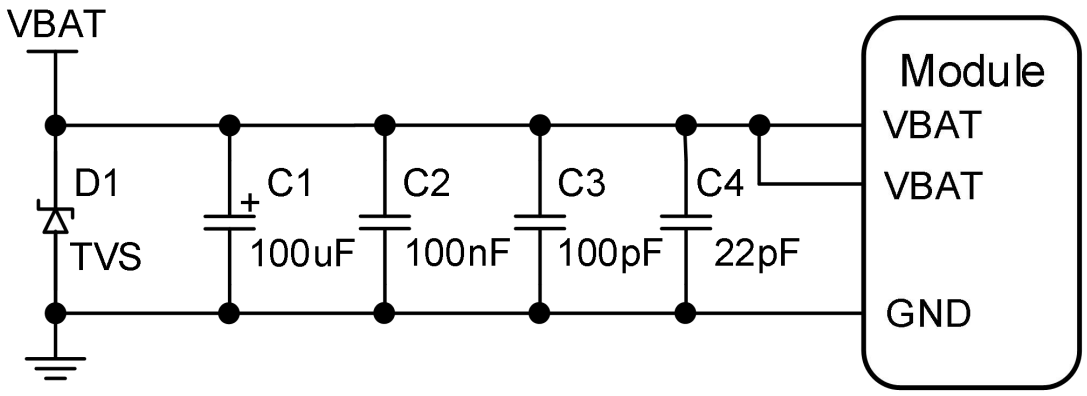


Figure 3-2 VBAT Input Reference Circuit

Power supply design has a significant impact on the performance of the module, it is important to choose a power supply that can provide at least 0.5A current capability.

If the voltage difference between the input voltage and the module's supply voltage is not significant, it is recommended to choose LDO as the power supply. If there is a large voltage difference between the input and output, then use DC-DC for power conversion, while paying attention to the EMI issues brought by DC-DC.

Ensure that the VBAT supply voltage input to the module does not fall below the minimum operating voltage of VBAT (pay attention to voltage drop issues). To ensure better power supply performance, the VBAT input terminal reference circuit is shown in the above figure. The longer the VBAT trace on the PCB design, the wider the trace width should be. It is recommended that the trace width should not be less than 1mm. The GND plane of the power supply section should be as complete as possible with multiple GND vias. Also, capacitors should be placed as close as possible to the VBAT pin of the module.

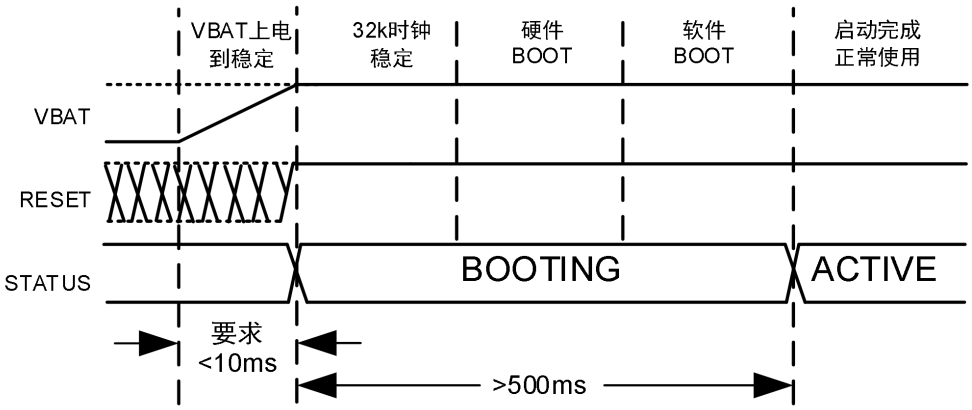
C1 is a 100uF tantalum capacitor with low ESR, which enhances the power supply's ripple current capability and stabilizes the voltage.

C2, C3, and C4 are 100nF, 100pF, and 22pF filter capacitors respectively, all in 0402 packages, used to eliminate high-frequency interference.

At the same time, it is recommended to add a TVS diode near the VBAT input to

improve the module's ability to withstand surge voltage.

3.4 Power on.



Timing diagram for Figure 3-3

Notes

◆ The initial state of VBAT when powered on needs to be less than 0.7V. If it is greater than 0.7V but less than 2.1V, it cannot guarantee that all power-on scenarios will be successful and the chip will work normally. The rise time of VBAT from 0V to 2.1V should be less than 10ms.

After VBAT power-off, it is necessary to ensure that the RESET voltage is below 0.35V. The specific discharge time needs to be evaluated based on actual circuit testing and with sufficient margin reserved to avoid abnormal startup when powered on again.

◆ RESET has weak pull-up internally, needs to be pulled up to high before the 32K clock stabilizes, so it is recommended to ensure that the RESET pin cannot be pulled low during the startup phase.

◆ The typical time for VBAT to power up to the module entering the Active state is >500ms. If the module's AT serial port outputs the word "Lierda," it indicates that the module has started up successfully.

◆ It is suggested that MCU retains the RESET control pin. In case of abnormal

power-on sequence leading to abnormal startup of the module, controlling the module to reset can exit the abnormal state.

3.5 Reset

The module is reset in the following way:

- Hardware reset: RESET pin, low level effective (pulling down to reset, time greater than 10ms).
- Software reset: send the "AT+ECRST" command to reset.

Table 3-4 Reset Pin Description

Pin number	Pin names	I/O	Description	Note
15	RESET	DI	Reset module	Low level effective

When the external control of the module RESET outputs a high level greater than 1.45V and less than 3.6V, and outputs a low level less than 0.35V, the RESET pin of the module can be directly connected for control. In other cases, an open-drain driver circuit must be used for control, as shown below.

3.5.1 Circuit reference design

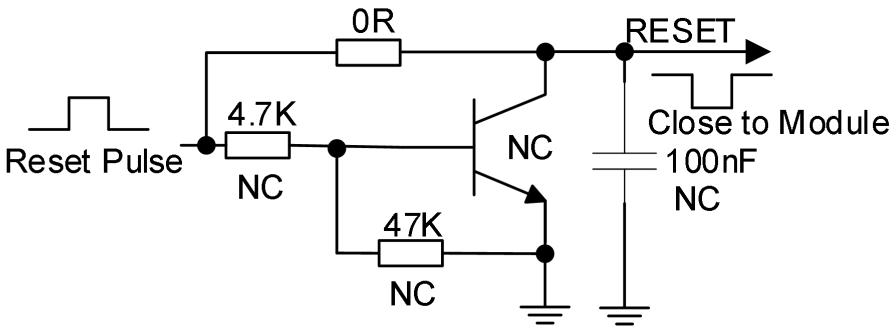


Figure 3-4 Transistor Reset Reference Circuit

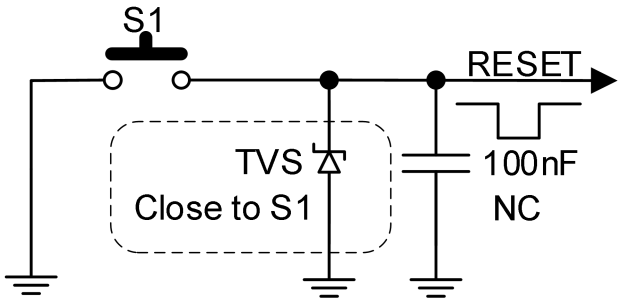


Figure 3-5 Key Reset Reference Circuit

Notes

During the reset process, both VBAT and the 32K clock need to be in a stable state.

◆ The RESET pin is effective when pulled low for more than 10ms.

◆ The reset line should not be too long, pay attention to grounding protection, keep away from RF, VBAT power sources, and strong signal interference sources, place the transistor as close as possible to the module RESET pin to avoid external signal interference.

◆ It is recommended to reserve a capacitor position of 100 nF~1μF at the RESET pin of the module by default without soldering.

3.6 Awaken

The module needs to be woken up through the PSM_EINT0 pin in PSM mode.

Table 3-5 Reset Pin Description

Pin number	Pin names	I/O	Description	Remark
19	PSM_EINT0	DI	External wake-up module	Low level effective

Note: In addition to waking up through the PSM_EINT0 pin, the module can also be woken up through the low-power serial port, please refer to section 4.1.1 for details.

3.6.1 Wake-up circuit reference design

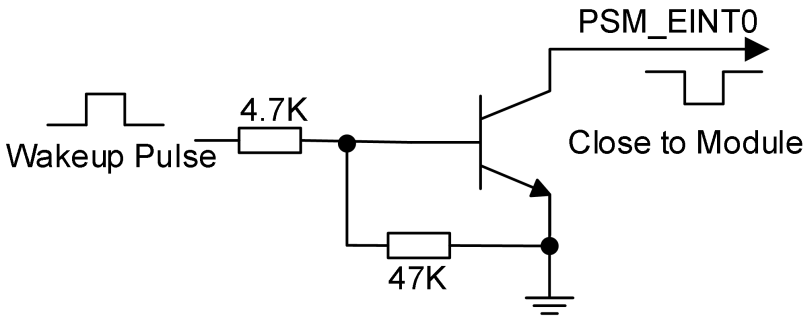


Figure 3-6 Transistor Wake-up Reference Circuit

Notes

During the wake-up process, VBAT/32K clock need to be in a stable state.

Lowering PSM_EINT0 (low level) can wake up the module from PSM.

◆ The wake-up line should not be too long, pay attention to grounding protection, stay away from RF, VBAT power sources and strong signal interference sources, place the transistor as close as possible to the module's PSM_EINT0 pin to avoid external signal interference.

4 Application interface

The MB26-A Y0C series module provides the following application interfaces:

◆Three UART interfaces

◆USIM interface all the way

◆Three-way GPIO interface

◆SPI interface all the way

◆Two ADC interfaces.

◆Ring signal RI※

◆Network status indicator NETLIGHT※

Note: "*" indicates that this feature is not supported by default and needs to be enabled by the software.

4.1 UART communication

The module provides three general asynchronous transceivers: main serial port, debug serial port, and application serial port. The baud rate of the main serial port can be configured as 4800bps/9600bps/115200bps/921600bps (firmware burning), the baud rate of the debug serial port is 3Mbps, only used for debugging, and the application serial port can be used normally for communication with peripherals.

Table 4-1 Serial Port Pin Definitions

Pin number	Pin names	I/O	Description	Note
17	MAIN_RXD	DI	Main Serial Port: Module receives data	Important: Under PSM, all serial ports except MAIN_RXD will be powered off.
18	MAIN_TXD	DO	Main serial port: Module sends data	
38	DBG_RXD	DI	Debugging serial port: Module receives data	
39	DBG_TXD	DO	Debugging serial port: Module sends data	

28	AUX_RXD	DI	Serial port application: Module receives data	
29	AUX_TXD	DO	Serial port application: Module sends data	

Notes

◆ The serial port interface belongs to the VO_LDOIO power domain, and the maximum voltage cannot exceed 3.6V.

◆ The VO_LDOIO power domain will power off in sleep mode, and MAIN_RXD will switch to the internal 1.2V power supply.

◆ The RXD pin of the serial port has an internal pull-up, so there is no need to connect an external pull-up resistor, and it has anti-backflow function.

◆ Pay attention to the consistency of the voltage levels when using the serial port, otherwise it may cause leakage current.

4.1.1 Main Serial Port

Main serial port characteristics:

- Used for AT command communication and data transmission, with a default baud rate of 9600bps.
- Configurable to 2400/4800bps/9600bps/115200bps* (*Not supported under PSM)
- Used for firmware upgrade, the baud rate is 921600bps during the upgrade.

The main serial port wakes up the low-power serial port, and in PSM mode, RXD will switch to the internal 1.2V power domain.

- The main serial port supports low-power serial port wake-up. In PSM mode, pulling RXD low will wake up the module, while VDD_EXT will be powered off in PSM mode, so VDD_EXT cannot be used as a pull-up.

The schematic diagram of the main serial port connection is as follows:

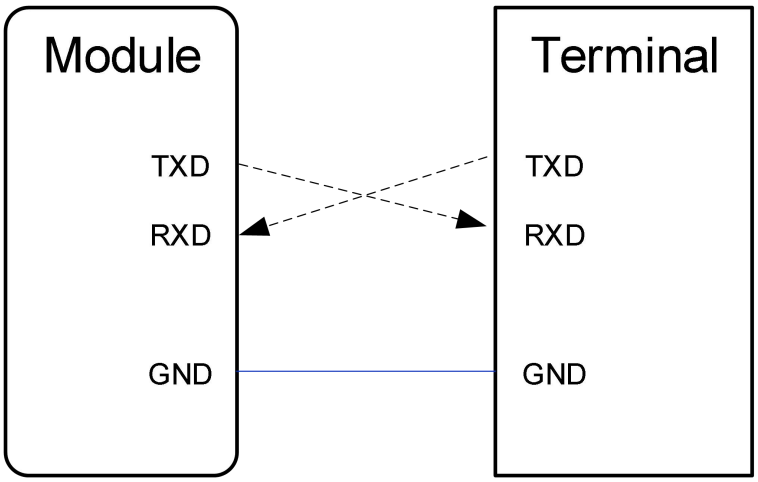


Figure 4-1 Main Serial Port Connection Diagram

4.1.2 Debug serial port

Characteristics of serial port debugging:

◆By using the dedicated tools provided by the platform, debugging the serial port to view log information for software debugging, with a baud rate of 3Mbps.

The schematic diagram of debugging the serial port connection is as follows:

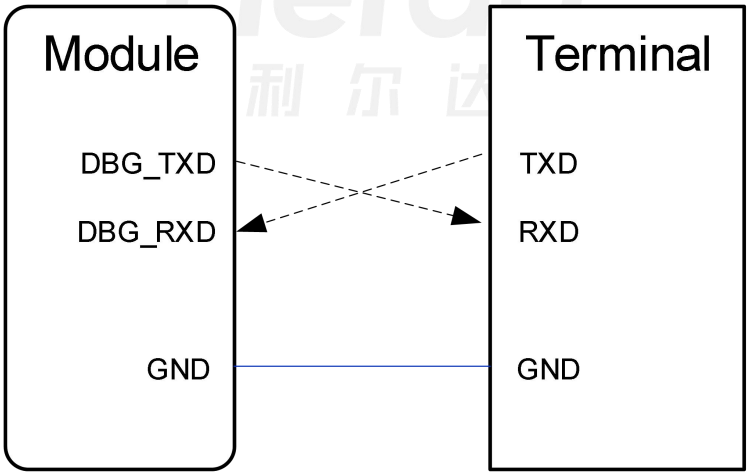


Figure 4-2 Schematic Diagram of Debugging Serial Port Connection

4.1.3 Serial Port Circuit Reference Design

The main considerations for a suitable serial port level conversion circuit include whether it meets the working speed of the serial port, scenarios with low power

requirements, and whether the power consumption meets the requirements. Below is a provided level matching circuit scheme for reference, choose or define according to the actual product requirements.

The RXD pin of the serial port has an internal pull-up resistor, external pull-up resistors are prohibited from being connected.

Typical level conversion reference circuit

This circuit has low cost and a wide range of applicable voltage levels (main control voltage levels from 1.8V to 5.0V can be used), but there are limitations on the serial port baud rate, with the maximum baud rate being 921600bps. The reference design is as follows, also pay attention to the direction of level conversion.

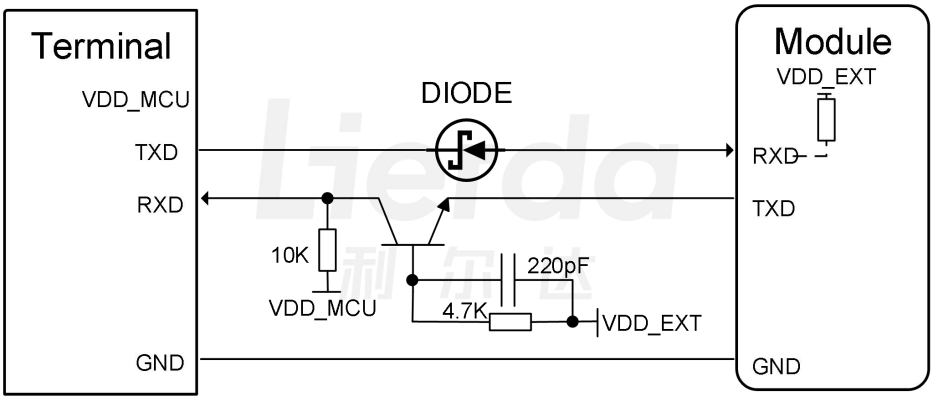


Figure 4-3 Level Conversion Reference Circuit

Recommendation of transistors for reference:

Brand: CJ Model: S8050 J3Y Package: SOT-23

Recommend Schottky diodes for reference (pay attention to the forward voltage of the diode):

Brand: LRC Model: LRB520S-30T1G Package: SOD-523

4.2 USIM card interface

The module includes an external USIM card interface, supporting the module to access the USIM card. The USIM card interface supports functions specified by 3GPP standards. The external USIM card is powered by the module internally, supporting cards powered by 1.8/3.0V.

Table 4-2 Definition of External USIM Card Interface Pins

Pin number	Pin names	I/O	Description	Note
11	USIM_DATA	IO	SIM card data cable	
12	USIM_RST	DO	SIM card reset line	
13	USIM_CLK	DO	SIM card clock line	
14	USIM_VDD	PO	SIM card power supply	Supports 1.8V/3V USIM card when 3.0V≤VBAT≤4.5V. Only supports 1.8V USIM card when 2.1V≤VBAT≤3V. Maximum supply current: about 30mA

4.2.1 USIM card circuit reference design

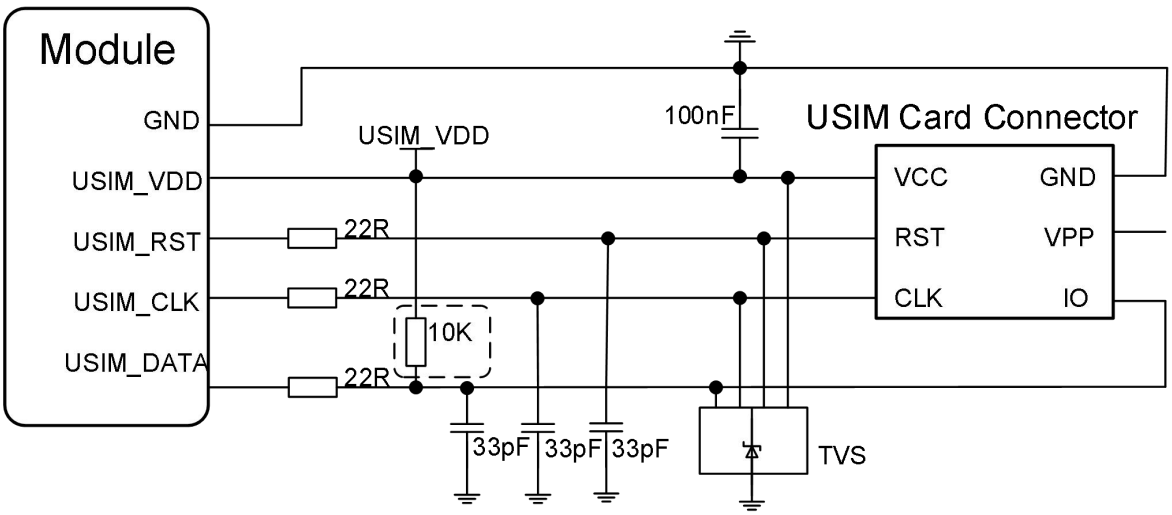


Figure 4-4 6PIN external SIM card reference circuit

4.2.2 Considerations for USIM card circuit design

To ensure the reliability and availability of the SIM card in applications, please read and follow the following standards for SIM card circuit design:

◆When laying out the board, try to place the SIM card as close to the module as possible, and keep the signal line routing length within 200mm if possible.

◆SIM card signal lines should be kept away from RF traces and VBAT power lines.

◆The GND wiring of the SIM card should be short and thick, ensuring that the wiring width is not less than 0.5mm. The decoupling capacitor of USIM_VDD should not exceed 1uF, and the capacitor should be placed close to the external SIM card's VCC.

◆To avoid signal interference between USIM_DATA and USIM_CLK, the wiring between the two should not be too close. Ground shielding should be added between the two traces. In order to prevent the negative effects of long traces, USIM_DATA generally needs to add a pull-up resistor to USIM_VDD to improve the driving capability. As there is a built-in pull-up resistor (10K) to USIM_VDD inside the module, if the traces are too long, it is recommended to externally reserve a 10K resistor placed near the card slot. In addition, the USIM_RST signal also needs to be ground protected.

◆The SIM card peripheral circuit should be close to the SIM card placement. To ensure good ESD protection performance, it is recommended to add TVS diodes to the pins of the external USIM card. The parasitic capacitance of the selected TVS diode should not exceed 15pF. ESD protection devices should be placed as close as possible to the external SIM card placement, and ensure that the protected SIM card signal lines pass through the ESD protection devices before reaching the module. A 22Ω resistor should be connected in series between the module and SIM card signal lines to suppress stray EMI and enhance ESD protection. In addition, a parallel 33pF capacitor is used to filter out RF interference.

4.3 General IO interface

The module provides two GPIO interfaces.

Table 4-3 GPIO Pin Definitions

Pin number	Pin names	I/O	Description	Note
7	GPIO0	IO	Internal connect GPIO0	
30	GPIO3	IO	Internal connect GPIO13	
31	GPIO4	IO	Internal connect GPIO14	

4.4 SPI interface

The module provides a SPI interface.

Table 4-4 SPI Pin Definitions

Pin number	Pin names	I/O	Description	Note
3	SPI_MISO	DI	SPI master input slave output	
4	SPI_MOSI	DO	SPI master output from input	
5	SPI_SCLK	DO	SPI serial clock	
6	SPI_CS	DO	SPI chip select	

4.5 ADC interface

Table 4-5 ADC Interface Pin Definitions

Pin number	Pin names	I/O	Description	Note
9	ADC0	AI	Universal Modulus Conversion	Internal direct connection Input voltage range: 0 to 1.6V
44	ADC1	AI	Universal Modulus Conversion	Internal voltage divider Input voltage range: 0~3.6V Default 1.6V Internal tap can be opened

				via software.

4.6 Ring signal RI※

When the URC information is reported, the module notifies the DTE through the RI pin. This function is not supported by default and needs to be enabled by software.

Table 4-6 RI signal status

Module Status	RI signal status
Standby	High level
URC	The new URC will have a low level of 120ms when returning to RI.

4.7 Network status indicator ※

NETLIGHT signals can be used to indicate the network status of the module. This function is not supported by default and needs to be enabled through software.

The reference connection circuit for the network status indicator is shown in the following figure:

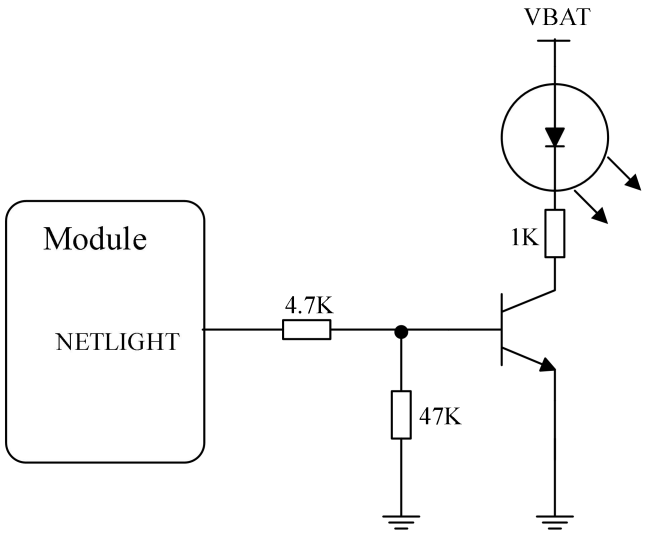


Figure 4-5 Network Indicator Light Interface Reference Circuit

5 Radio Frequency Characteristics

The module provides a NB-IoT RF interface, with a characteristic impedance of 50Ω.

5.1 Antenna interface and operating frequency band

ANT_RFIO is the RF antenna interface of the module, with a characteristic impedance of 50Ω. The frequency bands are Band3/5/8.

Table 5-1 RF antenna pin definitions

Pin number	Pin names	I/O	Description	Note
35	RF_ANT	IO	RF antenna interface, 50Ω characteristic impedance	

Table 5-2 RF Antenna Frequency Bands

Frequency band	Uplink frequency band	Downlink frequency band	Network standard
Band3	1710MHz-1785MHz	1805MHz-1880MHz	H-FDD
Band5	824MHz-849MHz	869MHz-894MHz	H-FDD
Band8	880MHz-915MHz	925MHz-960MHz	H-FDD

5.2 Transmit power

Table 5-3 Transmission Power

Frequency	Maximum value	Minimum value	Note
Band 5	23dBm±2.7dB	＜-40dBm	Compliant with NB-IoT protocol in 3GPP Rel-13 and Rel-14.
Band 8	23dBm±2.7dB	＜-40dBm	
Band 3	23dBm±2.7dB	＜-40dBm	

5.3 Sensitivity of reception

Table 5-4 Conduction reception sensitivity under single transmission (throughput ≥ 95%)

Frequency	Sensitivity reception	3GPP standards
Band3	-116.2dBm	-107.5dBm
Band5	-116.6dBm	-107.5dBm
Band8	-116.9dBm	-107.5dBm

Table 5-5 Conduction Reception Sensitivity under 128 Retransmissions (Throughput ≥95%)

Frequency	Sensitivity reception	
Band3	-134dBm	
Band5	-134dBm	
Band8	-134dBm	

5.4 Antenna circuit reference design

When using the module, a π-type matching circuit needs to be added between the RF antenna interface of the module and the antenna interface of the user's baseboard. The typical antenna matching circuit and initial parameters are shown in the figure below. The resistor is 0 ohms, the capacitor position is not mounted by default, and the recommended package for the components is 0201 or 0402.

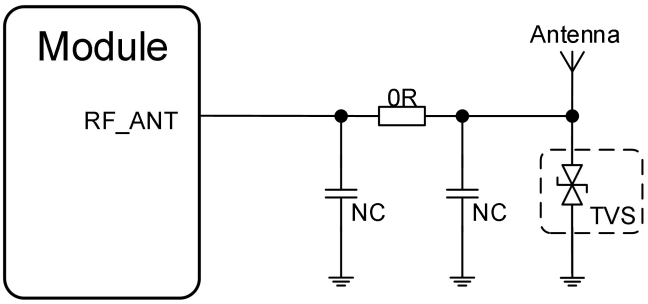


Figure 5-1 RF Antenna Reference Circuit

If an external antenna is used, or if users can touch the antenna, it is recommended to reserve a TVS tube to enhance electrostatic protection. Because the parasitic capacitance of the TVS may affect the antenna performance, it is recommended to re-adjust the antenna after adding the TVS tube.

The wiring requirements between RF_ANT and the user antenna must meet the 50Ω

RF characteristic impedance requirements. At the same time, the distance of the RF routing should be as short as possible to ensure minimal insertion loss of the RF routing. Detailed wiring requirements are provided in the following section.

5.5 RF signal line routing guide

- RF routing design requirements

The characteristic impedance of the RF signal line in the system applied by this module should be controlled at 50Ω. Generally, the impedance of the RF signal line is determined by the material's dielectric constant εr, trace width W, spacing to the GND D, and the thickness of the reference GND plane H. In the field of IoT applications, the design of PCB characteristic impedance is usually achieved through coplanar waveguide to help the RF signal line achieve better shielding and higher integration for compact design. The following diagram illustrates the structural requirements for PCB designs with different layers.

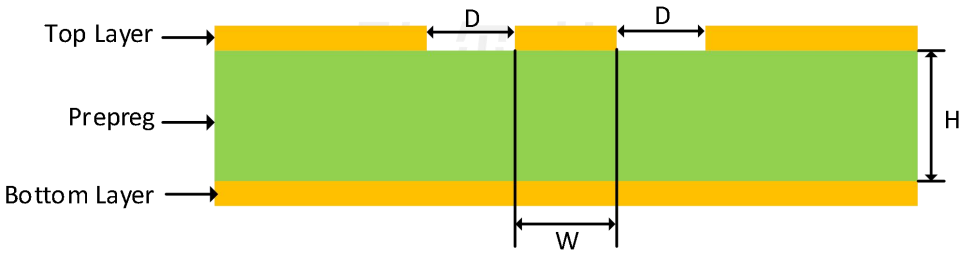


Figure 5-2 Two-layer PCB coplanar waveguide structure

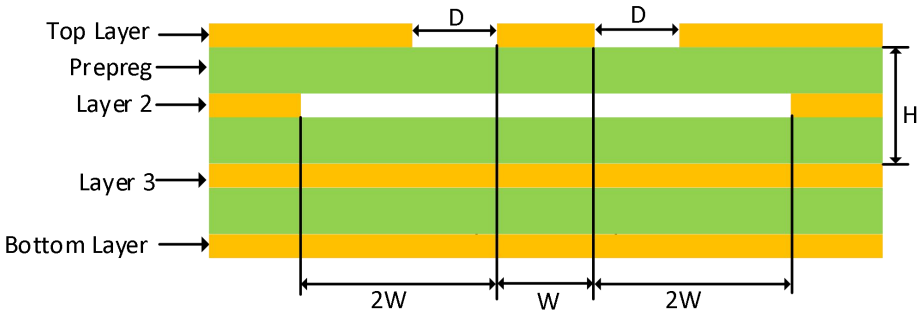


Figure 5-3 Four-layer PCB coplanar waveguide structure (reference ground is the third layer)

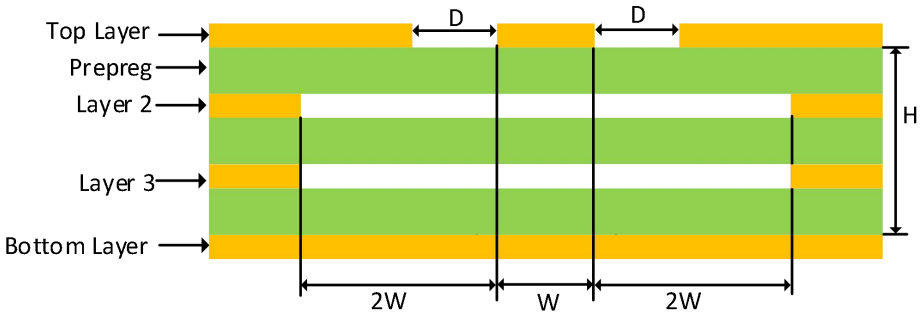


Figure 5-4 Four-layer PCB coplanar waveguide structure (reference ground is the fourth layer)

The control method of 50Ω impedance in Lierda design can be achieved using the Polar Si9000 design software tool. The calculation method in the figure below, taking the PCB finished thickness as 1.6mm as an example, can obtain the RF trace width W=0.65mm and the spacing between lines D=0.14mm.

Reference for the calculation method of 50Ω impedance in Figure 5-5

The following is a schematic diagram of the layout of the PCB RF circuit, with the following recommendations:

◆ Design according to the design results of the RF line width W and line spacing D.

◆ In the π circuit, three external matching reserved components are closely placed together. The reserved NC component can be placed on the same side or on both sides in the LAYOUT design (as shown in the figure).

◆ GND planes on both sides of the RF trace must have irregular through-hole VIAs placed to ensure that there are VIAs on the GND planes closest to the RF trace (as shown in the green boxed area in the diagram). There must be a complete GND plane below the entire RF trace space (as shown in the blue area in the diagram).

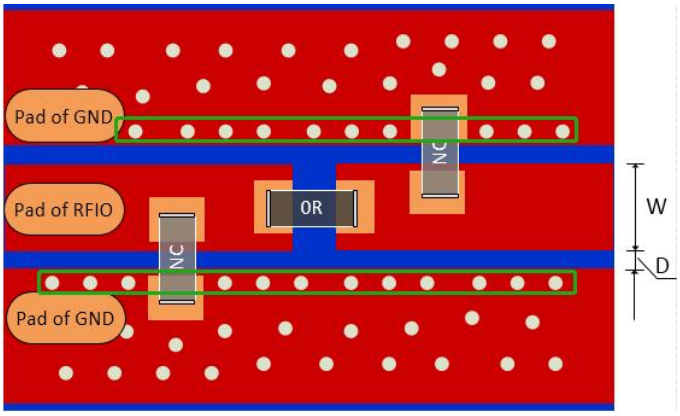


Figure 5-6 RF routing LAYOUT design schematic

◆ Wiring design guidance for modules in products

The reasonableness of RF routing can be directly reflected in the conduction test of the module, but in order to ensure the full performance of the product, antenna design cooperation is also required. In order to better meet the requirements of antenna design, the following requirements are hoped to be achieved in PCB design. Guidance will be provided for the whole machine PCB of different layers below:

When the PCB of the product is designed with 2 layers, it is best for both the TOP and BOTTOM LAYER directly below the module to be GND layers. The traces that need to be led out by the module should avoid running directly below the module and should be led out from the outer side of the module.

When the product PCB is designed with 4 layers, it is recommended that the traces that need to be led out by the module should be routed on the third or fourth layer, reserving the first and second layers for the module as complete GND reference layers.

5.6 Antenna design requirements

Module terminal antenna requirements: Select an antenna that meets the working frequency band of the module, with a characteristic impedance of 50Ω. The lower the insertion loss within the working frequency band, the better. The Voltage Standing Wave Ratio (VSWR) should be ≤2. The better the antenna performance, the higher the efficiency of the module, and the wider the coverage range.

5.7 Recommended RF connectors

Two common ways to connect the antenna:

◆Soldering of the pad: One end of the antenna is directly soldered to the antenna output port of the product using a high-frequency cable.

◆High-frequency head: using the connection method of SMA and IPX connectors, where the IPX connector is recommended to use Hirose's UF.L-R-SMT connector, IPX connector physical picture, SMA connector physical picture.

The types of antennas suitable for different NB-IoT scenarios are as follows, but not limited to:

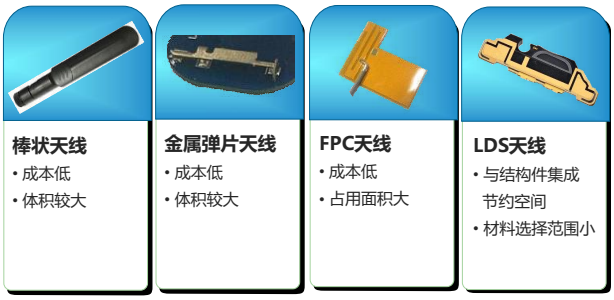


Figure 5-7 Recommended Types of Conventional Antennas for NB-IoT

6 Electrical performance and reliability

6.1 Absolute maximum rated value

Table 6-1 Maximum Rated Voltage of Pins

Pin types	Minimum value	Maximum value	Unit	Note
VBAT	-0.3	4.5	V	
Voltage at digital pins	-0.3	3.6	V	
Simulated voltage at the pin	-0.3	3.6	V	

6.2 Rated power value

Table 6-2 Power Interface Electrical Characteristics

Parameters	Description	Minimum value	Typical value	Maximum value	Unit
VBAT	Module normal supply voltage(1)	2.2	3.6	4.5	V
VBAT	Module expansion power supply voltage (2)	2.1	3.6	4.5	V
USIM_VDD	USIM card power supply output	-	1.8/3.0	-	V
VDD_EXT	Reference power output (3)	-	1.8/3.0/3.3	-	V

Notes

(1) When the module operates within this voltage range, the module's relevant performance meets the 3GPP standard requirements.

(2) When the module operates within this voltage range, it can still maintain normal operation without irreparable faults; only individual indicators, such as output power and other parameter values, may exceed the range of the 3GPP standard. When the voltage returns to the normal operating range, all indicators of the module still comply with the 3GPP standard.

The specific description of the VDD_EXT voltage is shown in Table 2-4.

6.3 Power consumption

Table 6-3 Module Current Consumption

Pattern	Description	Frequency band	Typical value	Unit
PSM	Sleep mode @3.6V		1.5	uA
Idle	Idle state DRX (1.28s), ECL0@3.6V		270	uA
	Idle state DRX (2.56s), ECL0@3.6V		135	uA
Active Launch	RF transmission status Single-tone(15 kHz) (23dBm)@3.6V	B3	275	mA
		B5	231	mA
		B8	222	mA
	RF transmission status Single-tone(15 kHz) (12dBm)@3.6V	B3	98	mA
		B5	55	mA
		B8	55	mA
	RF transmission status Single-tone(15 kHz) (0dBm)@3.6V	B3	31	mA
		B5	27	mA
		B8	26	mA
Active Receive	RF receiving status ECL0 @3.6V	B3	3.3	mA
		B5	3.5	mA
		B8	4.8	mA

6.4 Digital logic voltage characteristics

Table 6-4 1.8V I/O Logic Level Characteristics

Parameters	Description	Minimum value	Maximum value	Unit
VIH	Input high level	0.7 x VDDIO	-	V

VIL	Low level input	-	0.2 x VDDIO	V
VOH	Output high level	0.8 x VDDIO	-	V
VOL	Low level output	-	0.15 x VDDIO	V

Table 6-5 USIM card 1.8V logic level characteristics

Parameters	Describe	Minimum value	Maximum value	Unit
USIM_VDD	Power supply	1.7	1.9	V
VIH	Input high level	0.7 x USIM_VDD	-	V
VIL	Low level input	-	0.2 x USIM_VDD	V
VOH	Output high level	0.8 x USIM_VDD	-	V
VOL	Low level output	-	0.15 x USIM_VDD	V

Table 6-6 USIM card 3.0V logical level characteristics

Parameters	Description	Minimum value	Maximum value	Unit
USIM_VDD	Power supply	2.85	3.15	V
VIH	Input high level	0.7 x USIM_VDD	-	V
VIL	Low level input	-	0.2 x USIM_VDD	V
VOH	Output high level	0.8 x USIM_VDD	-	V
VOL	Low level output	-	0.15 x USIM_VDD	V

6.5 Static electricity protection

Electrostatic protection instructions:

In module applications, static electricity generated by human static electricity, electrostatic friction between microelectronics, and discharged to the module through various ways may cause certain damage to the module. Therefore, ESD protection should be emphasized. In the process of research and development, production assembly, testing,

etc., especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the interface of circuit design and points vulnerable to static discharge damage or interference; testing equipment should ensure good grounding; anti-static gloves should be worn during production.

Table 6-7 ESD performance parameters (Temperature: 25℃, Humidity: 45%)

Pin name	Discharge	Unit
VBAT,GND	±8	kV
Antenna interface	±8	kV
Other interfaces	±0.5	kV

6.6 Work and storage temperature

Table 6-8 Working Temperature Range

Parameters	Minimum value	Typical value	Maximum value	Unit	Note
Operating temperature(1)	-40	+25	+85	℃	
Storage environment temperature(2)	-40	+25	+90	℃	

Notes

(1) When the module operates within this temperature range, the module's relevant performance meets the requirements of the 3GPP standard.

(2) This storage temperature range does not include packaging materials, attention should be paid to the maximum temperature tolerance of the tape packaging.

6.7 Notes

During the production and use of modules, there are some points to pay attention to:

◆ When spraying the module, please try to avoid the spraying material flowing into the interior of the module;

◆ When cleaning the module, do not use ultrasonic cleaning on the module, as it may cause damage to the internal crystals of the module.

◆ When producing and using modules, please avoid applying them in environments or enclosures containing any amount of mercury or mercury vapor, as this may lead to the risk of product failure or malfunction.

7 Mechanical dimensions

7.1 Mechanical dimensions

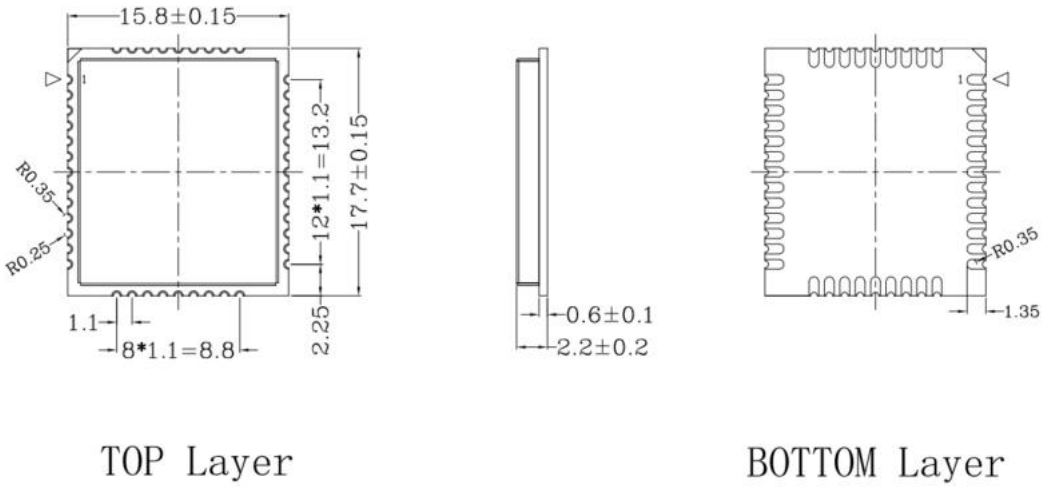


Figure 7-1 Module Mechanical Dimensional Drawing

7.2 Module top view / bottom view

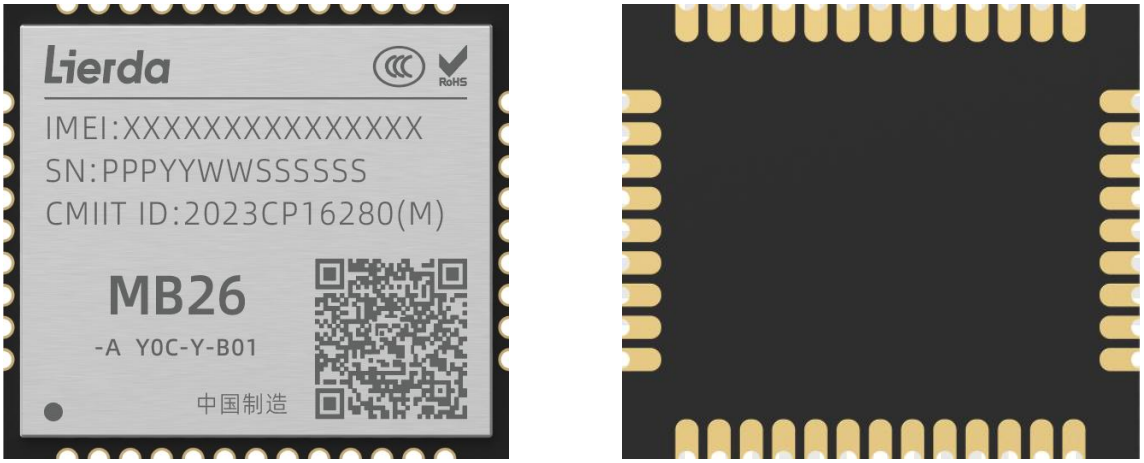


Figure 7-2 Module Top/Bottom View

The above is the design rendering of the module. Please refer to the actual module for accuracy, especially the label content is for reference only. For more information, such as

module packaging recommendations, production guidelines, and packaging methods, please refer to our production guide document.

7.3 Recommendation for packaging

The module recommends solder pads as shown in the following figure, and users can make minor adjustments according to their own production processes.

- The pins around the module are designed with right angles. When designing the solder pads on the user's board, consider using rounded corners for smooth transition. The square solder pads on the bottom of the module can be designed with the module pin dimensions, as shown in the reference design diagram below.
- To facilitate the opening of the ladder steel mesh, it is recommended not to layout other components within a 2.0mm range outside the module solder pad. Users can refer to the requirements of their own steel mesh manufacturers to determine this distance.

Note: The module pads are symmetrically distributed around the module center point.

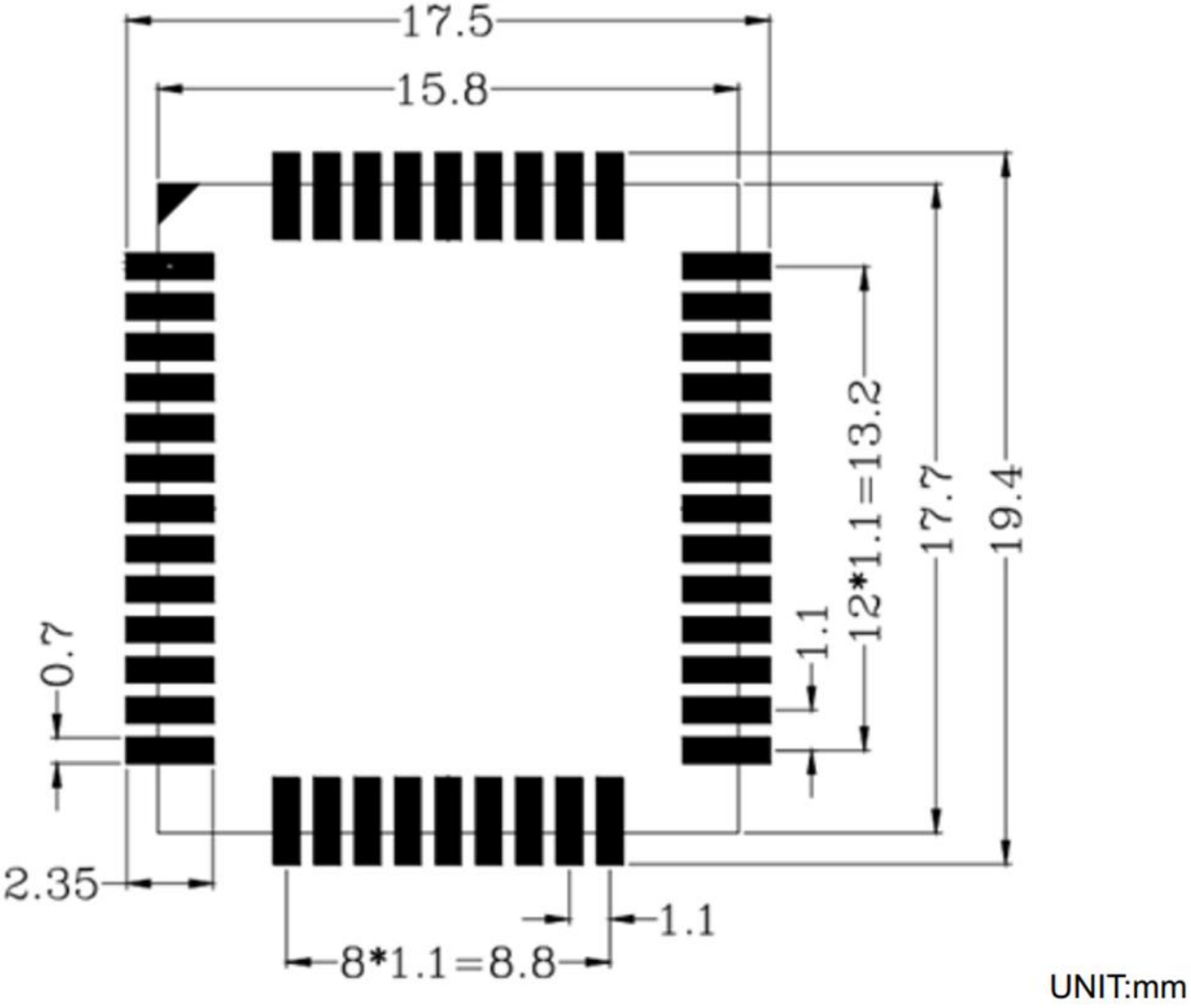


Figure 7-3 Module Recommended Solder Pads

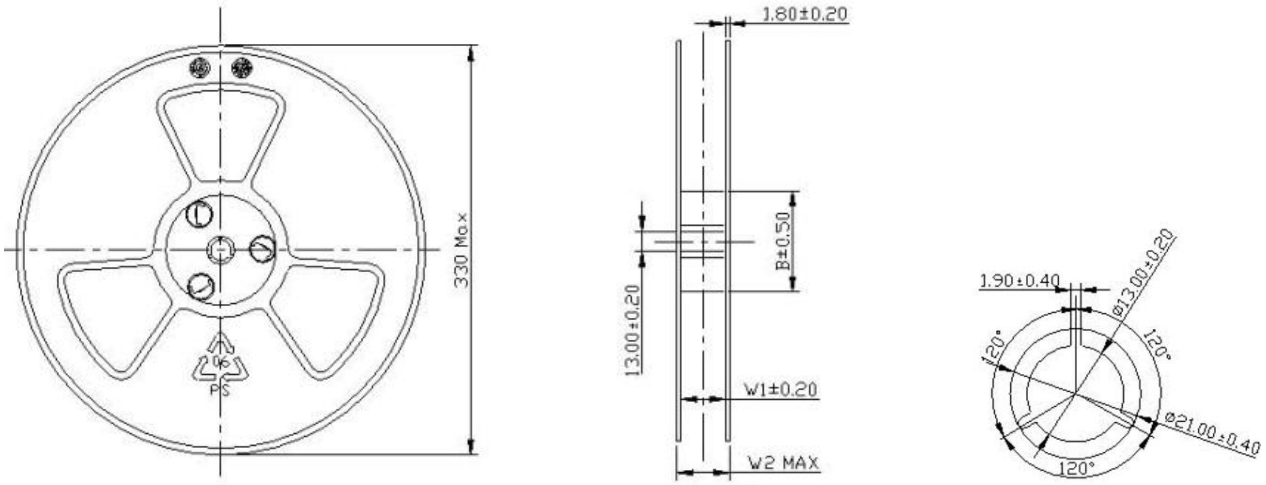
8 Packaging and production information

This chapter describes guidance information on the packaging, storage, production, maintenance, etc. of modules, which is applicable to the assembly process guidance of modules.

8.1 Packaging specifications

The factory packaging of this module uses a rubber wheel carrying method, the

reference dimensions of the rubber wheel are as follows:



Reel Size(mm)			
Tape Width	B±0.5	W1±0.2	W2 Max
32	100	32.4	38.4

The loading direction is as follows: (Refer to the diagram, the actual content of the label shall prevail, pay attention to the position of module PIN1)

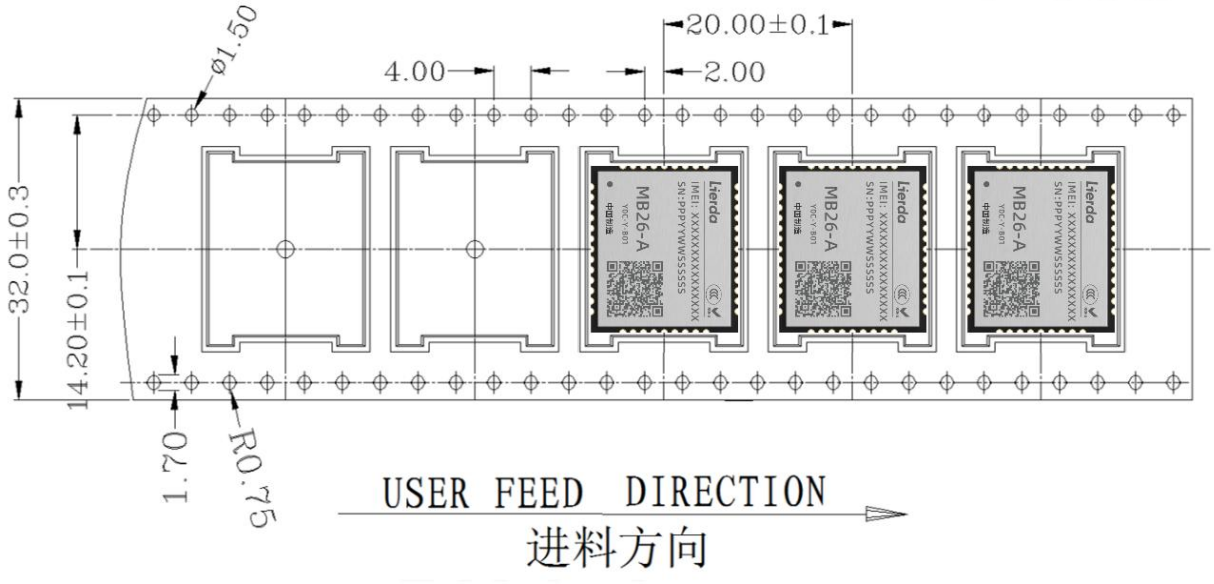


Figure 8-1 Packaging Specifications and Dimensions

8.2 Storage Conditions

The modules are shipped in the form of vacuum reel sealed bags, with a moisture sensitivity level of MSL 3.

Storage conditions:

1) When the temperature is below 40°C and the humidity is below 90% (RH), the solderability can be guaranteed for 12 months in well-sealed packaging.

After unpacking, ensure surface mounting assembly within 168 hours under the condition of ambient temperature below 30°C and relative humidity below 60% (RH).

If the above conditions are not met, baking is required:

1) Rolled tape packaging, baked at 60℃±5℃ for 24-48 hours,

If acceleration of baking is needed, the module should be taken out from the tape and placed on a high-temperature resistant container (e.g. tray) for baking (ESD protection should be observed during the removal process), baked at 125°C ±5°C for 8 hours.

3) The cumulative baking time cannot exceed 96 hours.

Refer to the IPC/JEDEC J-STD-033 standard for more detailed guidance.

8.3 Manufacturing welding

8.3.1 Furnace charging method

If the customer uses a double-sided board for the module's baseboard, it is recommended to place the module in the second reflow. It is best for the customer's baseboard to go through the oven on the carrier tape during the first reflow, and also try to place it on the carrier tape during the second reflow. If for special reasons it cannot go through the oven on the carrier tape, consider using a fixture to go through the oven on the track or place a flat, high-temperature resistant flat board under the PCBA to support it during reflow to prevent PCB deformation leading to virtual soldering of the module during reflow.

8.3.2 Reflow soldering operation guidance

The PCBA reflow soldering temperature curve is related to the use of solder paste and

needs to be adjusted according to the actual solder paste. The data is only suitable for lead-free operations, refer to Figure 8-2 Lead-free Reflow Soldering Operation Guide.

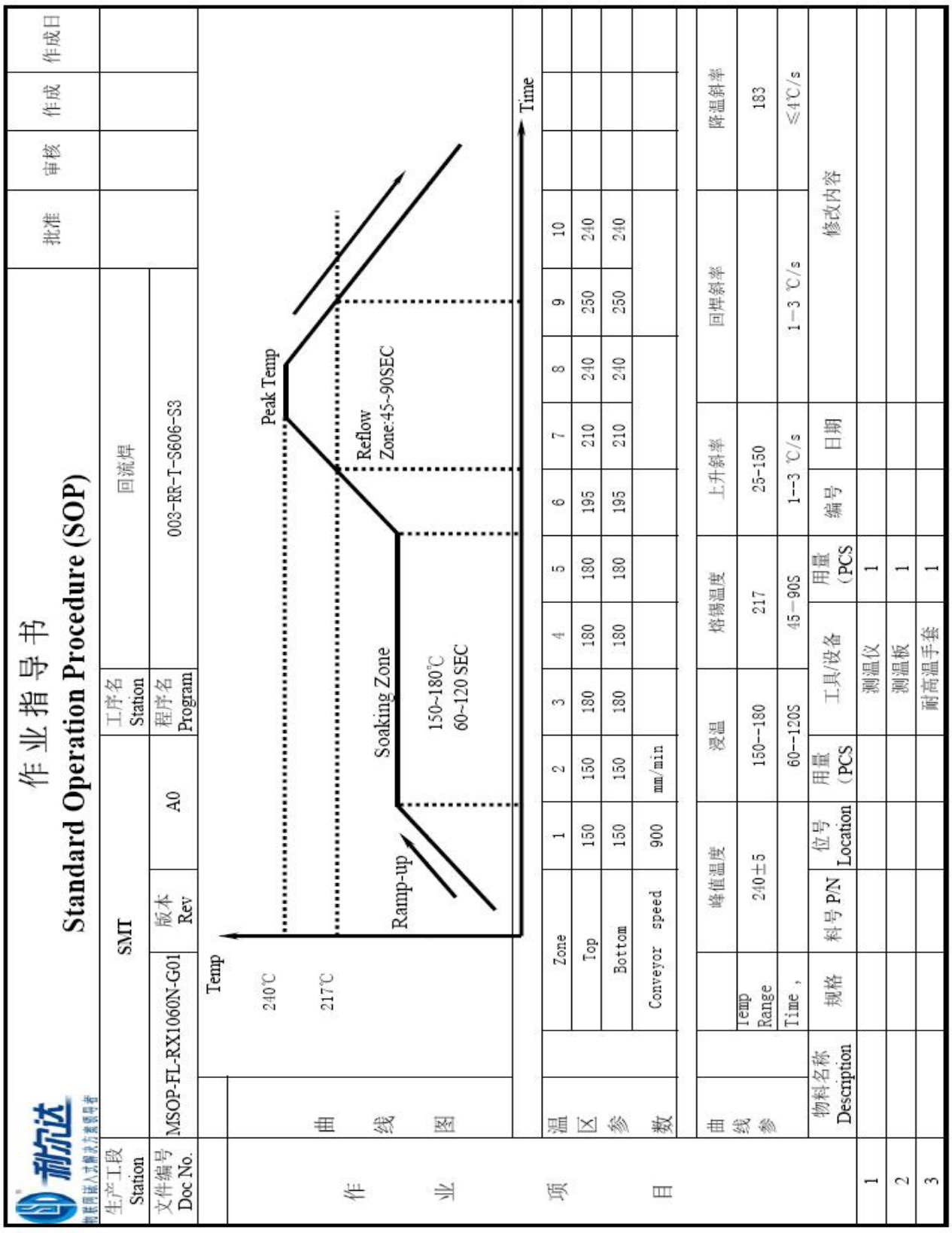


Figure 8-2 Lead-Free Reflow Soldering Operation Guide

8.3.3 Production process

During the production welding or any other process that may directly contact the module, do not use any organic solvents (such as alcohol, isopropanol, acetone, trichloroethylene, etc.) to wipe the module shield; otherwise, it may cause the shield to rust.

If spraying or potting is needed for the module, please ensure that the spraying or potting materials used will not chemically react with the module shield or PCB, and also make sure that the spraying or potting materials will not flow into the interior of the module.

When producing and using modules, please avoid applying them in environments or packaging containing any amount of mercury or mercury vapor, as this may lead to the risk of product failure or malfunction.

8.3.4 Repair

If the module has defects such as virtual welding or short circuit that require repair, please follow the parameters below:

Lead-free process: Soldering iron temperature 380±10℃, soldering iron contact time ≤5S;

Lead process: Soldering iron temperature 350±10℃, soldering iron contact time ≤5S;

Modules are not recommended to be blown with a hot air gun to avoid affecting the performance of the module.

9 Related documents and terminology abbreviations

9.1 Related documents

The following documents provide the names of the documents, please refer to the latest release for the version.

Table 9-1 Related Documents

Serial number	Document Name	Annotation
[1]	IPC/JEDEC J-STD-033 specification	

9.2 Term abbreviation

Table 9-2 Term Abbreviations

Abbreviation	Full name in English	Full Chinese name
3GPP	3rd Generation Partnership Project	The Third Generation Partner Program
ADC	Analog-to-Digital Converter	Analog-to-Digital Conversion
ANT	Antenna	Antenna
DAC	Digital -to- Analog Converter	Analog-to-Digital Conversion
DBG-	Debug	Debugging
DC-DC	Direct Current - Direct Current	DC converter
DCXO	Digitally Controlled Crystal Oscillator	Digital Controlled Crystal Oscillator
DRX	Discontinuous Reception	Non-continuous reception
DTE	Data Terminal Equipment	Data terminal equipment
ECL	Equivalent Class Level	Network coverage level
ESD	Electro-Static discharge	Electrostatic discharge

EOS	Electrical Overtress	Electrical super stress (surge)
ESR	Equivalent Series Resistance	Equivalent series resistance
EVK	Evaluation Kit	Evaluation toolkit
H-FDD	Half Frequency Division Duplexing	Frequency Division Duplex (FDD)
FOTA	Firmware Over-The-Air	Remote firmware upgrade
GPIO	General-purpose input/output	Common input and output
I/O	Input/Output	Input output interface
Imax	Maximum Load Current	Maximum current
Inorm	Normal Current	Normal (typical) current
bps	Bits Per Second	Units of speed
LCC	Leadless Chip Carriers	Leadless chip carrier packaging
LDO	Low Dropout Regulator	Low dropout linear regulator
LGA	Land Grid Array	Grid array packaging
LwM2M	Lightweight Machine-To-Machine	Lightweight M2M protocol
MCU	Mirco Controller Unit	Microcontroller
MSL	Moisture Sentivity levels	Humidity sensitivity level
NB-IoT	Narrow Band Internet of Things	Narrowband Internet of Things
PCB	Printed Circuit Board	Printed Circuit Board
PCBA	Printed Circuit Board Assembly	Printed Circuit Board Components
PMU	Power Management Unit	Power Management Unit
PSM	Power Saving Mode	Energy-saving mode
RF	Radio Frequency	Radio Frequency
RoHS	Restriction of Hazardous Substances	Limitation of harmful substances
RXD	Receive external Data	Receive
TAU	Tracking Area Update	Track area update
TCP/IP	Transmission Control Protocol/Internet Protocol	Transmission Control

		Protocol/Internet Protocol
TVS	Transient Voltage Suppressor	Transient Voltage Suppression Diode
TXD	Transmit external Data	Send
UART	Universal Asynchronous Receiver & Transmitter	General asynchronous receiver and transmitter
UDP/IP	User Datagram Protocol - Internet Protocol	User Datagram Protocol
USIM	Universal Subscriber Identification Module	Universal User Identification Module
VSWR	Voltage Standing Wave Ratio	Voltage Standing Wave Ratio
Vmax	Maximum Voltage Value	Maximum voltage
Vnorm	Normal Voltage Value	Normal (typical) voltage
Vmin	Minimum Voltage Value	Minimum voltage
VIHmax	Maximum Input High Level Voltage Value	Maximum input high level
VIHmin	Minimum Input High Level Voltage Value	Minimum input high level
VILmax	Maximum Input Low Level Voltage Value	Maximum input low level
VILmin	Minimum Input Low Level Voltage Value	Minimum input low level
VImax	Absolute Maximum Input Voltage Value	Maximum input level
VImin	Absolute Minimum Input Voltage Value	Minimum input level
VOHmax	Maximum Output High Level Voltage Value	Maximum output high level
VOHmin	Minimum Output High Level Voltage Value	Minimum output high level
VOLmax	Maximum Output Low Level Voltage Value	Maximum output low level
VOLmin	Minimum Output Low Level Voltage Value	Minimum output low level